WHAT IS CLAIMED IS:

1. A reconfigurable chip comprising:

a multiplication block including at least one multiplication unit and a group of selectable adder units operably connected to the multiplication unit, wherein the adder units are selectively connectable in different configurations; and

interconnect elements operably connected to the multiplication block, the interconnect elements adapted to selectively connect together the multiplication block with other reconfigurable units.

2. The reconfigurable chip of Claim 1 wherein the multiplication block further comprises input multiplication multiplexers for the block.

3. The reconfigurable chip of Claim 2, wherein there are fewer block input multiplexers than input multiplexers for the multiplication units.

4. The reconfigurable chip of Claim 1 wherein the adder units include input multiplexers.

5. The reconfigurable chip of Claim 1 wherein the multiplication units include input multiplexers.

6. The reconfigurable chip of Claim 1 wherein there are multiple multiplication units in each block.

7. The reconfigurable chip of Claim 1 wherein the instruction configures the multiplexers in the multiplication block.

8. The reconfigurable chip of Claim 1 wherein the multiplication block includes registers associated with the multiplication unit and adder units.

9. The reconfigurable chip of Claim 1 wherein the other type of unit is operably connectable to the adder units and can be used instead of multiplier units.

10. The reconfigurable chip of Claim 9 wherein the other type of unit comprises the despreader/correlator unit.

11. The reconfigurable chip of Claim 1 wherein the adder units can be connected together into chains.

12. The reconfigurable chip of Claim 1 wherein the interconnect elements are adapted to transfer word length data.

13. The reconfigurable chip of Claim 1 wherein further comprising an instruction memory storing multiple instructions for the reconfigurable functional units.

14. The reconfigurable chip of Claim 13 wherein a state machine addresses the instruction memory.

15. The reconfigurable chip of Claim 1 wherein the multiplication block includes a selectable output register for the multiplier units and the adder units.

16. The reconfigurable chip of Claim 1 wherein the multiplication block includes at least two multiplication units.

17. The reconfigurable chip of Claim 1 wherein the multiplication block includes at least four multiplication units.

18. A reconfigurable chip including:

a multiplication block including at least one input multiplexer, a multiplication unit operably connected to the input multiplexer, a group of selectable adder units operably connected to the multiplication unit, wherein the adder units are selectively connectable in different manners; and

an instruction memory storing multiple instructions for the multiplication block.

19. The reconfigurable chip of Claim 18 wherein there are input multiplexers for the block.

20. The reconfigurable chip of Claim 18 wherein there are input multiplexers associated with the adder units.

21. The reconfigurable chip of Claim 18 wherein there are input multiplexers for the multiplication unit.

22. The reconfigurable chip of Claim 18 wherein there are fewer block input multiplexers and then input multiplexers for the multiplication units.

23. The reconfigurable chip of Claim 18 wherein there are multiple multiplication units in each block.

24. The reconfigurable chip of Claim 23, wherein there are at least four multiplication units in each multiplication block.

25. The reconfigurable chip of Claim 18 wherein the multiplication block includes a decoder to decode a portion of the instruction.

26. The reconfigurable chip of Claim of 18 wherein the multiplication block includes registers associated with the adders units and multiplication units.

27. The reconfigurable chip of Claim 26 wherein the registers of selectable output registers.

28. The reconfigurable chip of Claim 18 wherein another type of unit is operably connectable to the adders and can be used instead of the multiplier unit.

29. The reconfigurable chip of Claim 28 wherein the other type of unit is a despreader/correlator unit.

30. The reconfigurable chip of Claim 18 wherein the adder units can be connectable into a chains.

31. The reconfigurable chip of Claim 18 further comprising interconnect units operably connected to the multiplication block.

32. The system of Claim 18 wherein the instruction memory is addressed by a state machine.

33. A reconfigurable chip including:

a multiplication block including at least one input multiplexer, a multiplication unit operably connected to the input multiplexer, a group of selectable adder units operably connected to the multiplication unit, wherein the adder units are selectively connectable in different manners; and

an instruction memory storing multiple instructions for the multiplication block.

34. The multiplication block of Claim 33 wherein there are fewer block input multiplexers than input multiplexers for the multiplication units.

35. The multiplication block of Claim 33 wherein there are at least four multiplication units in each multiplication block.

36. The reconfigurable chip of Claim 33, wherein there are four multiplication units in each multiplication block.

37. The reconfigurable chip of Claim 33 wherein the multiplication blocks are configured by an instruction.

38. The reconfigurable chip of Claim 37 wherein at least portions of the instruction is sent to a decoder in the multiplication block.

39. The system of Claim 33 wherein the multiplication block includes registers in the multiplication block to store output values.

40. The multiplication block of Claim 39 wherein the registers are selectable output registers.

41. The multiplication block of Claim 33 wherein there is another type of unit operably connected to the adder units strictly used instead of the multiplier unit.

42. The system of Claim 40 wherein the other type of unit comprises a despreader/correlator unit.

43. The multiplication unit block of Claim 33 wherein the adder units can be arranged into a chain.

44. The multiplication block of Claim 33 further associated with interconnect elements adapted to transfer data between the multiplication block and other local elements.

45. The multiplication block of Claim 33 further including an instruction memory storing multiple instructions for the reconfigurable functional units.

46. The multiplication block of Claim 45 further comprising a state machine addressing the instruction memory.

47. A multiplication block on a reconfigurable chip, the multiplication block including:

multiple block input multiplexers;

at least two multiplication units, each multiplication unit associated with two multiplication input multiplexers, the multiplication input multiplexers operably connected to the multiple block input multiplexers; and

a group of selectable adder units with associated adder input multiplexers, the adder input multiplexers operably connected to the multiplication units.

48. A reconfigurable chip comprising:

a multiplication block including at least one multiplication unit and a group of selectable adder units operably connected to the multiplication unit, wherein the adder units are selectively connectable in different configurations; and

reconfigurable functional units operably connectable to the multiplication block, the reconfigurable functional units including an arithmetic logic unit and a shifter unit units.